REMARKS

Reconsideration of the application is requested.

Claims 1-76 remain in the application. Claims 1-38 are subject to examination and claims 39-76 have been withdrawn from examination. Claims 1 and 20 have been amended.

In item 3 of the above-identified Office Action, claims 1-7, 10, 11, 13-26, 29, 30 and 32-38 have been rejected as being obvious over U.S. Patent No. 6,598,148 to Moore et al. in view of U.S. Patent No. 6,134,707 to Herrmann et al. under 35 U.S.C. § 103.

Applicant respectfully traverses the rejection. In addition, applicant has amended the claims to even further distinguish the invention from the prior art.

Let us first consider the teaching in Moore et al. With regard to the application-specifically configurable intelligent interface defined in claims 1 and 20, the Examiner has referred to column 14, lines 62-67 and column 15, lines 1-20 of Moore et al. The cited portions merely teach that the I/O interface 432 is operated in both an asynchronous mode and a synchronous mode by using a dual clock scheme. With regard to the application-specifically configurable intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements defined in claims 1 and 20, the Examiner has referred to column 4, lines 1-11, column 14, lines 62-

67 and column 15, lines 1-20 of Moore et al. The cited portion in column 4 merely teaches that the microprocessor 50 includes a CPU 70, an ALU 80, a stack 74, and registers 76, 78. The cited portion in column 4 does not in any way relate to an interface, and certainly does not teach an interface with structurable data paths or structurable logic elements. As already discussed, the cited portions in columns 14 and 15 merely teach that the I/O interface 432 is operated in both an asynchronous mode and a synchronous mode by using a dual clock scheme.

Claims 1 and 20 have been amended to further distinguish the invention from the I/O interface 432, which is taught by Moore et al., and which is merely operated in both an asynchronous mode and a synchronous mode. Support for the changes can be found by referring to the deleted portions of claims 1 and 20, and to the specification at page 11, line 9 through page 12, line 4, and at page 19, lines 4-14, for example.

Claims 1 and 20 now define an application-specifically configurable intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements, <u>said structurable data paths and/or said structurable logic elements being structurable to provide a plurality of different data paths for connecting said intelligent core and said plurality of units and/or for connecting at least some of said plurality of units to each other</u>.

The I/O interface 432, which is taught by Moore et al., and which is operated in both an asynchronous mode and a synchronous mode by way of a dual clock scheme, does not include structurable data paths and/or structurable logic elements that are structurable to provide a plurality of different data paths for connecting an intelligent core and a plurality of units together and/or for connecting at least some of a plurality of units to each other. There is no teaching that the I/O interface 432 has different structurable data paths for connecting different peripheral units or memory devices to each other or to an intelligent core.

Moore et al. do not teach or suggest the limitations of claims 1 and 20, which have been copied above. Therefore, even if there were a suggestion to combine the teachings of Moor et al. and Herrmann et al., for some reason, the claimed invention would not have been obtained.

With regard to the alleged motivation to combine the teachings of Moore et al. and Herrmann et al., applicant respectfully reminds the Examiner that MPEP 706.02(j) (D) specifies that the Examiner must provide an explanation as to why the claimed invention would have been obvious to one of ordinary skill in the art at the time the invention was made. In that regard the Examiner has stated that the motivation to combine the teachings of Moore et al. and Herrmann et al. "would have been to programming IC containing programmable elements". Applicant assumes that the Examiner meant to say that the motivation would have been to program an IC containing programmable elements. The

"invention" taught in Herrmann et al. is a method and device for programming integrated circuits that contain programmable elements (column 3, lines 20-29). See column 1, line 17-column 3, line 19 for a discussion of the prior art. Herrmann et al. achieve their goals by defining a new APL program language (column 4, lines 47-48). The entire teaching in Herrmann et al. is directed towards programming programmable IC's in general.

The Examiner has referred to column 23, lines 52-67 of Herrmann et al. to support the stated motivation for combining the cited references. The Examiner stated that the motivation would have been to program an IC containing programmable elements. Column 23, lines 62-65 of Herrmann et al. simply teach that their invention can be used with any type of IC with programmable elements. The motivation put forth by the Examiner seems to be circular and is not believed to be a valid motivation since Moore et al. do not even teach an IC with programmable elements. Is it the Examiner's reasoning that since Herrmann et al. teach a method of programming a programmable IC, then it would have been obvious to configure particular programmable elements in an application-specifically configurable intelligent interface of a program-controlled unit? If so, applicant respectfully asserts that the Examiner's reasoning is flawed and that a legitimate reason for combining the references has not been put forth. The mere fact that Herrmann et al. teach a method of programming a programmable IC does not provide a motivation for configuring particular programmable elements in an application-specifically configurable intelligent interface of a program-controlled unit.

In item 20 of the above-identified Office Action, claims 8, 9, 12, 27, 28, and 31 have been rejected as being obvious over U.S. Patent No. 6,598,148 to Moore et al. in view of U.S. Patent No. 6,134,707 to Herrmann et al. and further in view of U.S. Patent No. 5,825,878 to Takahashi et al. under 35 U.S.C. § 103.

Even if Takahashi et al. does teach what the Examiner alleges and even if there were a suggestion to combine the teaching of Takahashi et al. with that of Moore et al. and Herrmann et al., the invention as defined by these rejected claims would not have been obtained for the reasons given above with regard to claims 1 and 20.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or claim 20.

In view of the foregoing, reconsideration and allowance of claims 1-38 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the

amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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